Introduction to Faults

DFT Unit 2

KRKSastry

Terminology

- Controllability The ability to apply test patterns to the inputs of a sub-circuit via the primary inputs of the circuit.
- Double-throw switch Single pole double throw (SPDT) switch
- Logic Equality Checker(LEC) looks at the combinatorial structure of the design to determine if the structure of two alternative implementations will exhibit the same behavior
- Observability The ability to observe the response of a sub-circuit via the primary outputs of the circuit or at some other output pins.

- Test state Register and Controlled Incorporated in the design, could be a shift register that is Loaded by just a few signals
- Tri-state Buffer
- Scan-in , Scan-out Scan signals

Introduction

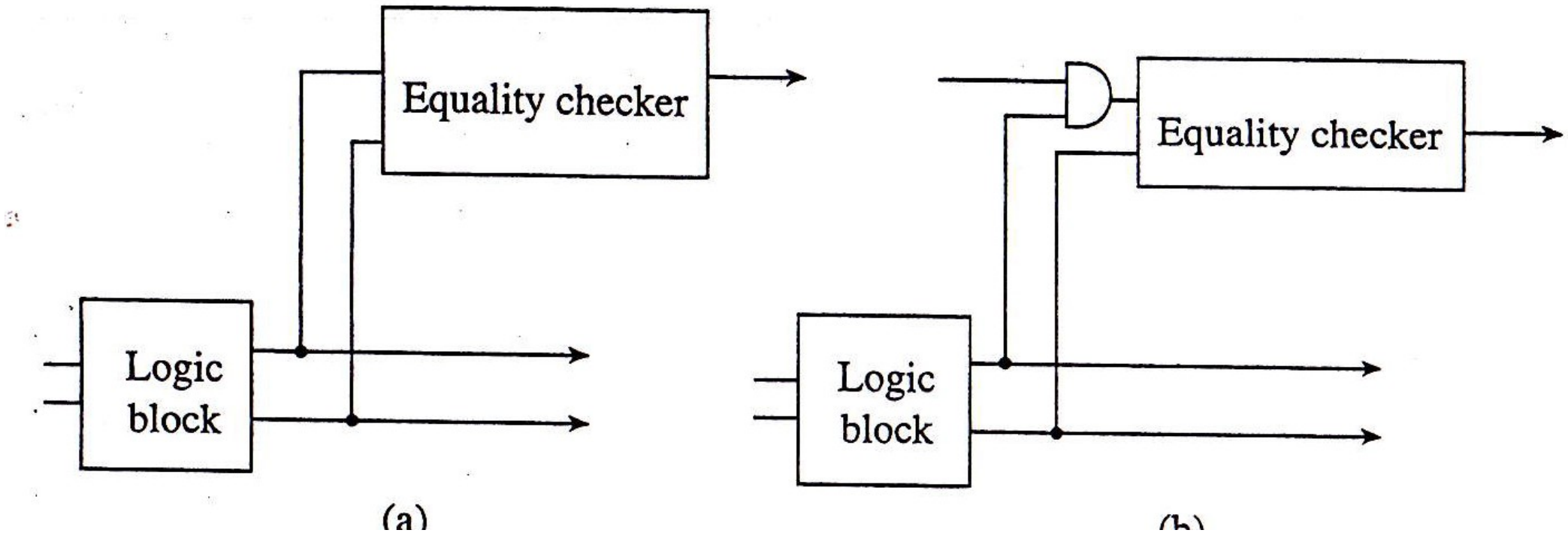
- Test generation for sequential circuits is significantly more complex than that for combinational circuits.
- Many design guidelines have been proposed to improve the testability of sequential circuits by adding extra test points;
- However, these involve non-systematic (i.e., ad hoc) design modifications and depend heavily on a designer's ingenuity.
- Scan design methodology A well-established approach to solve testability problem for sequential circuits is to constrain the design in a way that provides direct access to the memory elements in a circuit.
- It is widely used in designing sequential circuits with enhanced testability.

Controllability and Observability

- There are Two key concepts in designing for testability: controllability and observability.
- Controllability refers to the ability to apply test patterns to the inputs of a sub-circuit via the primary inputs of the circuit.
  - Ex: if the output of the Equality checker circuit is always in the state of equal, it is not possible to test whether the equality checker is operating correctly or not. (Figure a)

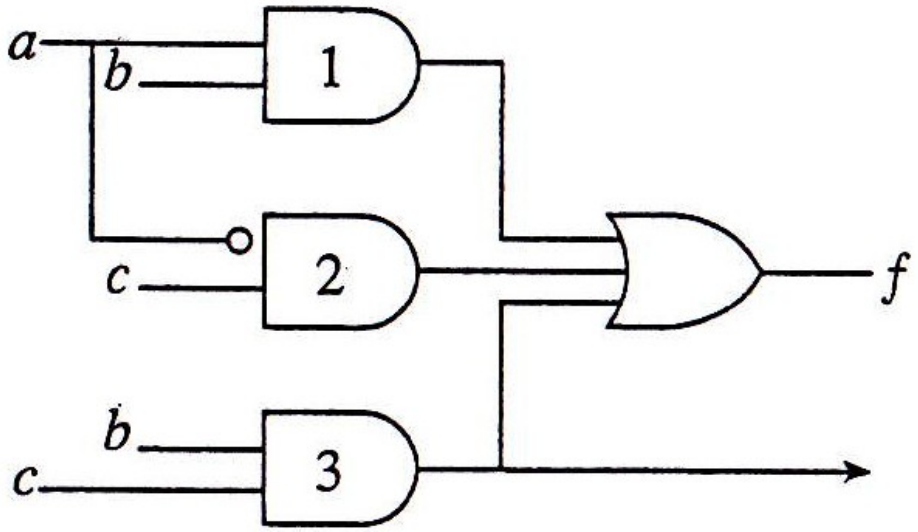
- If a control gate is added to the circuit, the input of the Equality checker can be controlled . Hence the operation of the circuit can be controlled.
- Therefore, to enhance the controllability of a circuit, the state that cannot be controlled from its primary inputs has to be reduced (Figure b).

Controllability and Observability contd ..



Observability

- Observability refers to the ability to observe the response of a sub-circuit via the primary outputs of the circuit or at some other output pins.
  - Ex: in the below figure, the outputs of all three AND gates are connected to the inputs of the OR gate. A stuck-at-0 fault at the output of the AND gate 3 is not detectable because the effect of the fault is masked and cannot be observed at the primary output.
- To enhance the observability, we must observe the output of the gate separately as shown.
- In general, the controllability /observability of a circuit can be enhanced by incorporating some cor l by adding some output lines (observabi



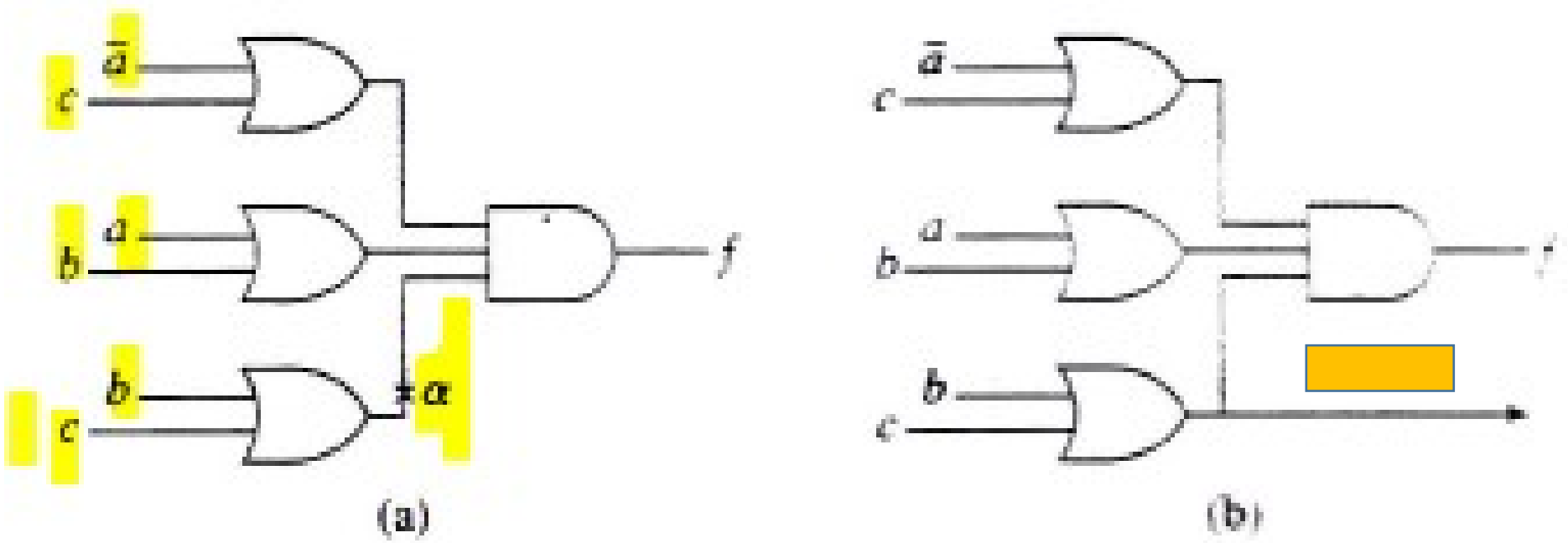
Ad hoc design rules for improving Testability

Ad hoc rules are used to improve testability of specific circuits.

1. Incorporate an additional control / Gate and observation points in a circuit.
2. Incorporating a two input multiplexer.
3. Use a Tristate driver.
4. To permit access to a subset of the Logic.

Additional Control added – Extra output point

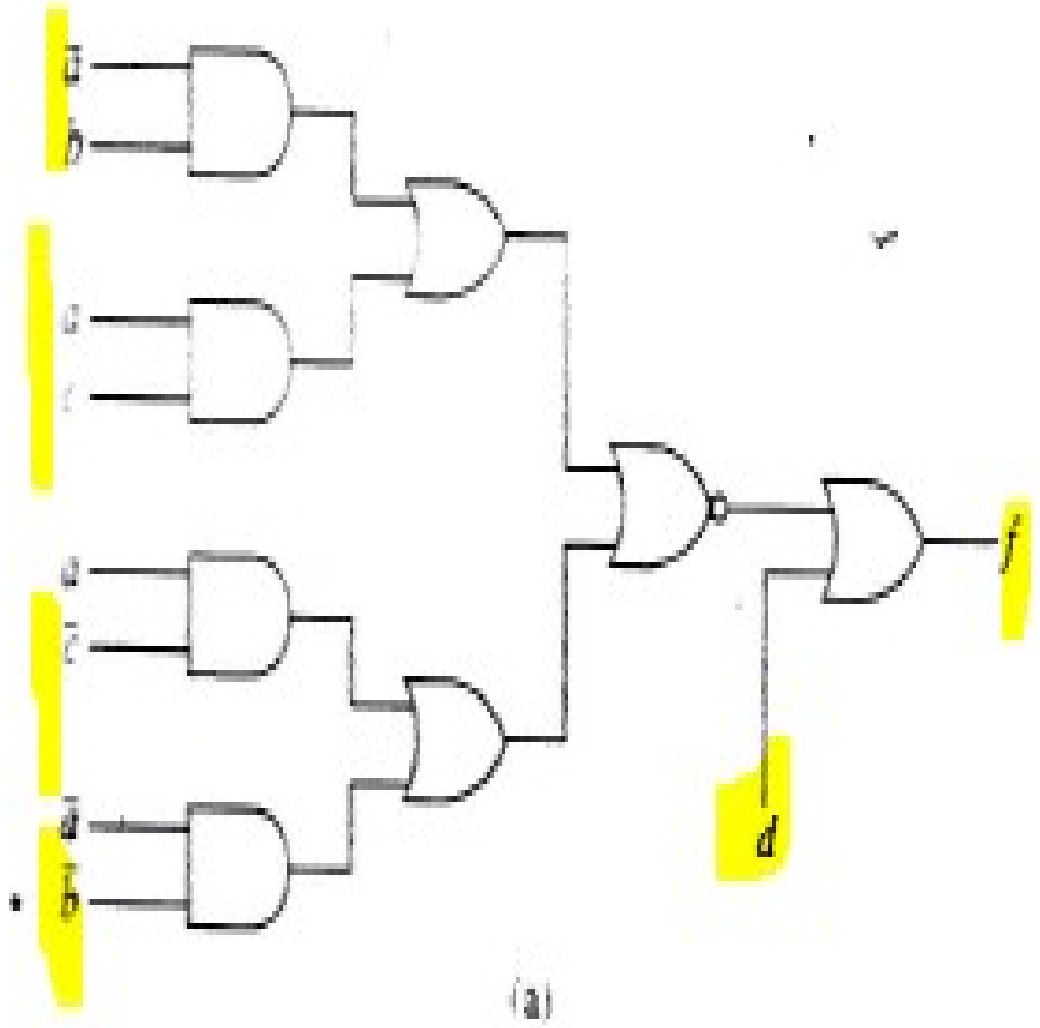
- Ad hoc rules are used to improve testability of specific circuits- One of the simplest ways of achieving this is to incorporate an additional control, and observation points in a circuit.
  - Ex: α s-a-1 fault in the below Figure –a, is undetectable at the circuit output.
  - To detect the fault, b=0; and c=0;
  - in such a case output from the top two OR gates is a and respectively. So, the output f=0;
  - Addition of an extra output line in the circuit makes the fault detectable Figure –b.



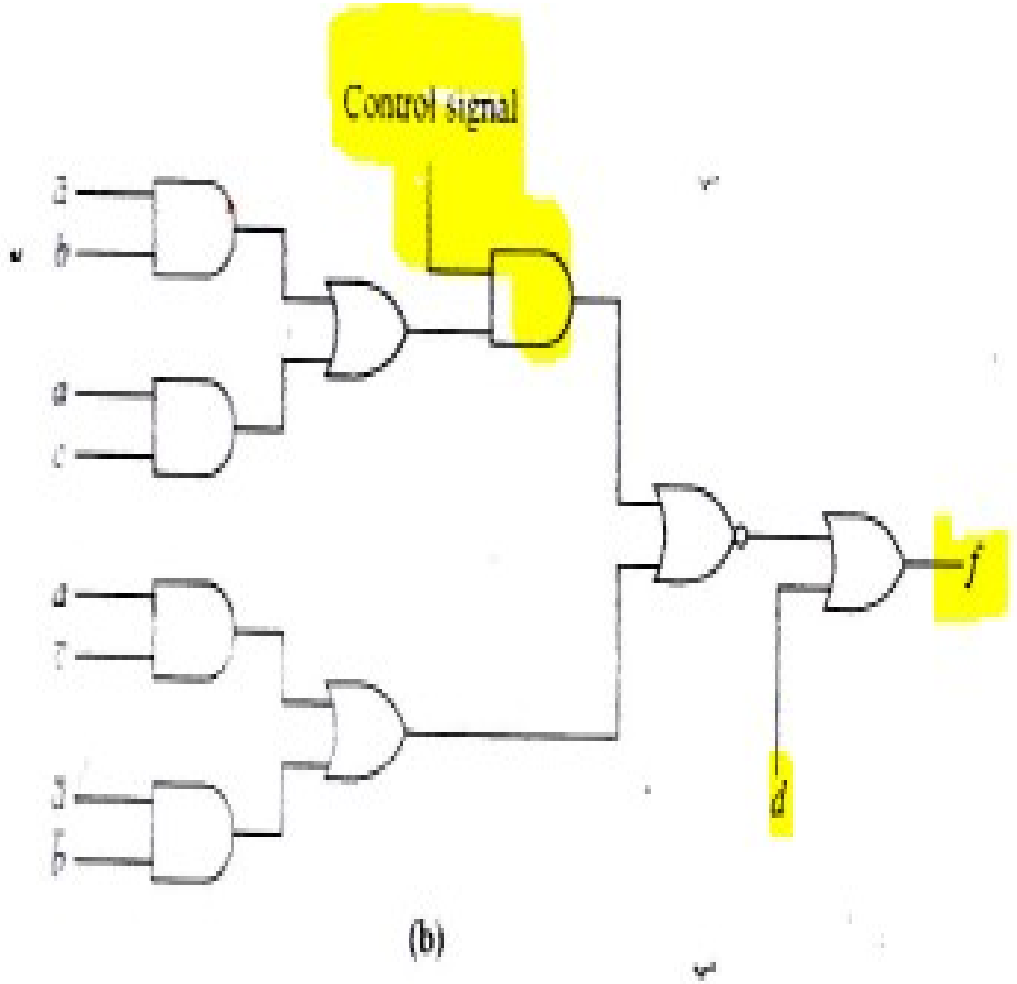
Additional Control added – Extra AND gate

- The usefulness of inserting a control point can be understood from the circuit shown in Figure-a (Slide 10)
- The output of the NOR gate is always 0 !! (any combination of a, ,b c makes one of the below set makes NOR gate input as high, so the output is always Zero)
  - b + ac are inputs to top set of gates
  - a + are input to the bottom set of gates
  - So, it is not possible to determine whether the gate is functioning correctly or not. (Y to use such circuit ??)
- If a control point is added (AND gate) to the circuit as shown in Figure-b (next Slide) , the NOR gate can be easily tested for single stuck-at fault

Additional Control added – Extra AND gate contd ...



(a)



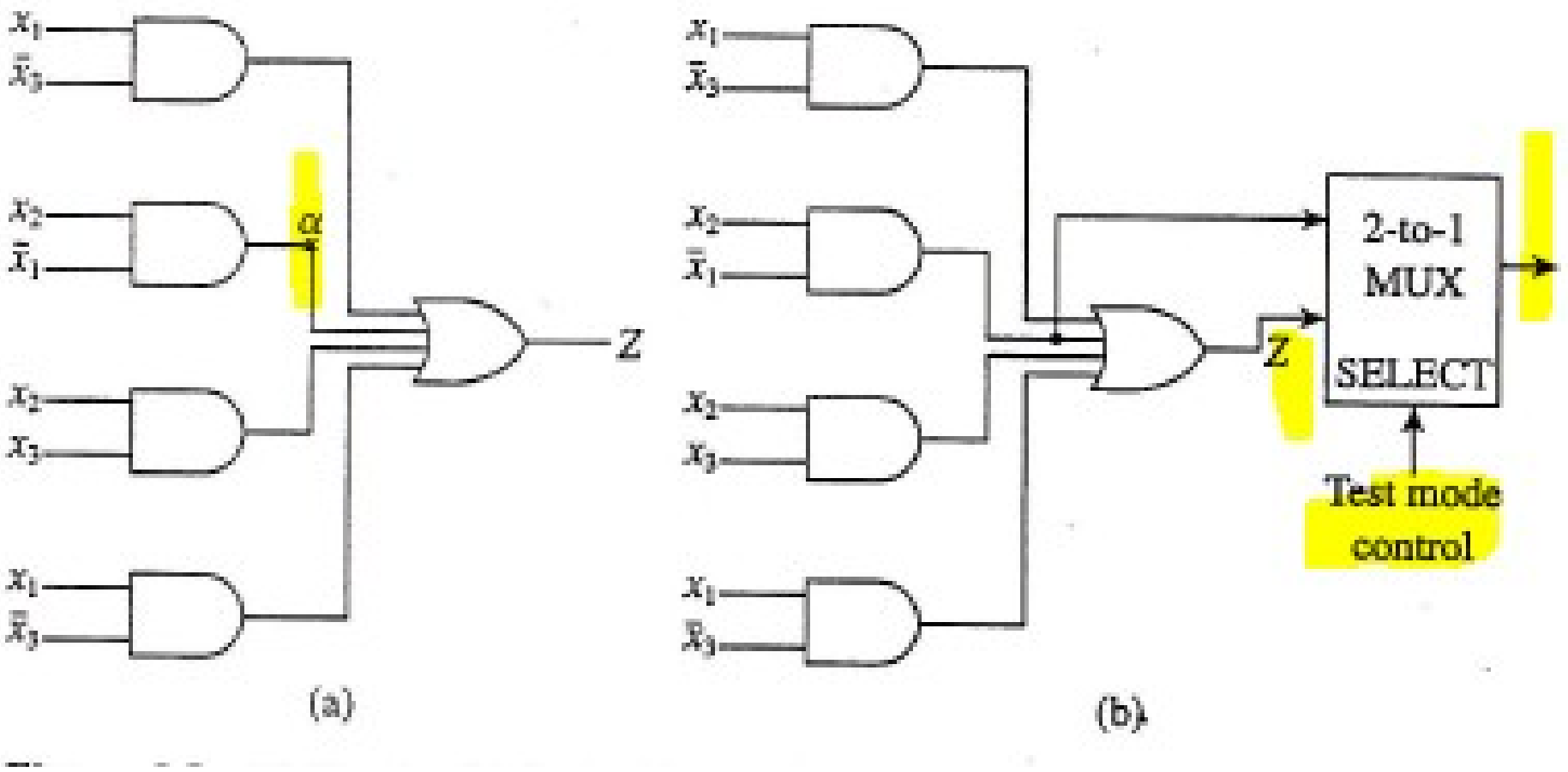
(b)

Additional Multiplexers added

- Another way of testability is to insert multiplexers to increase the number of Internal Points that can be controlled or observed from the external pins.
  - EX:
  - α s-a-1 fault is undetectable at the primary output Z Figure-a (Slide 12).
  - To detect α s-a-1 fault =0 and or x2=0 ;
  - In the case =1 ; x2=0 (x1 =0, X2 =1); All the gates output is Zero. So, α s-a-1 fault can be detected.
  - Top and Bottom Gates have the same set of Inputs !!

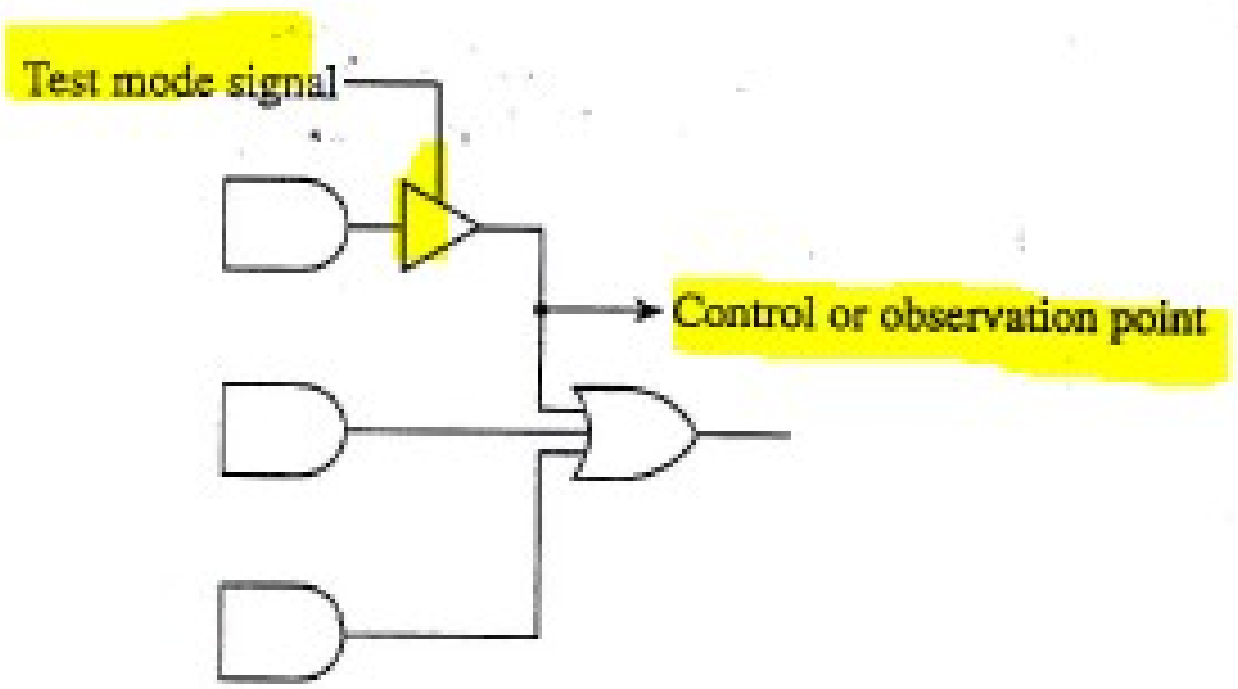
- By incorporating a multiplexer as shown in Figure-b, the input combination 010 can be applied to detect the fault via the multiplexer circuit.

Additional Multiplexers added contd ..



Use a Tristate driver

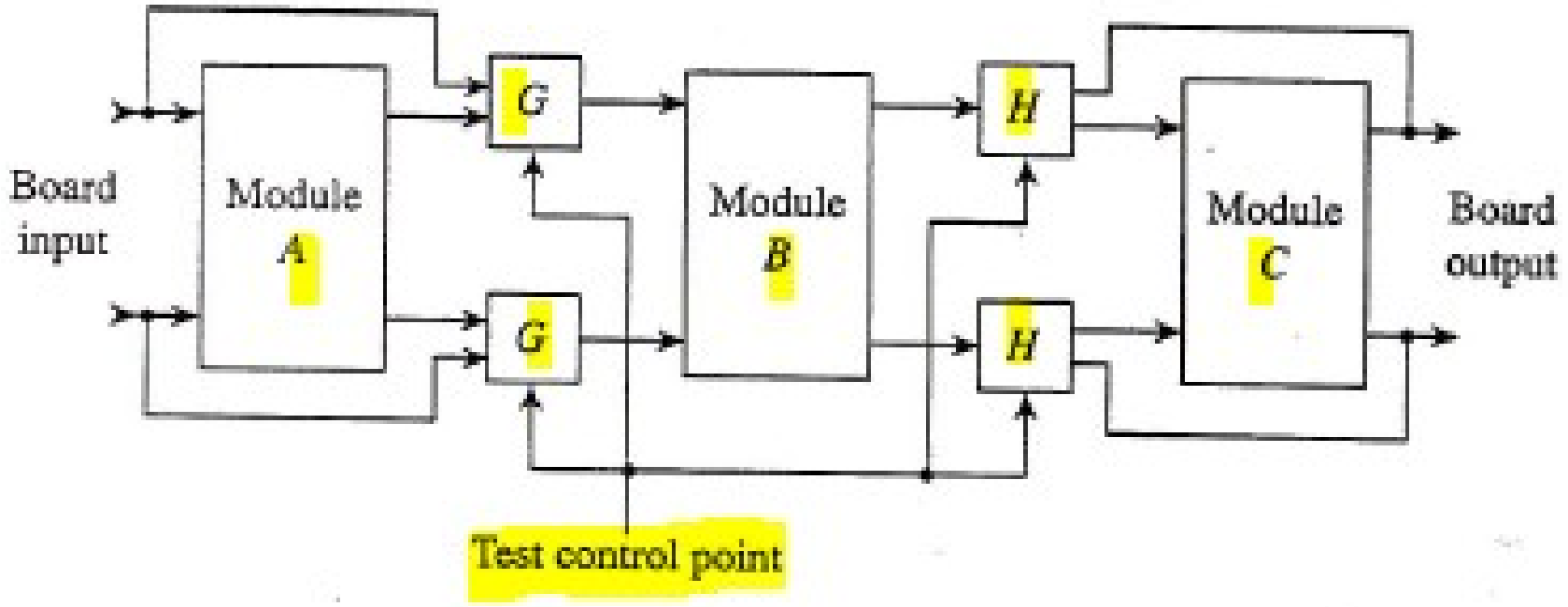
- Achieving access to internal points is to use a Tristate drivers.
- A test mode signal could be used to put the driver in to the high impedance state.
- In this mode the internal point could be used as a control point. When the driver is activated, the Intenal point becomes a test point.



To permit access to a subset of the Logic using Mux and De-mux

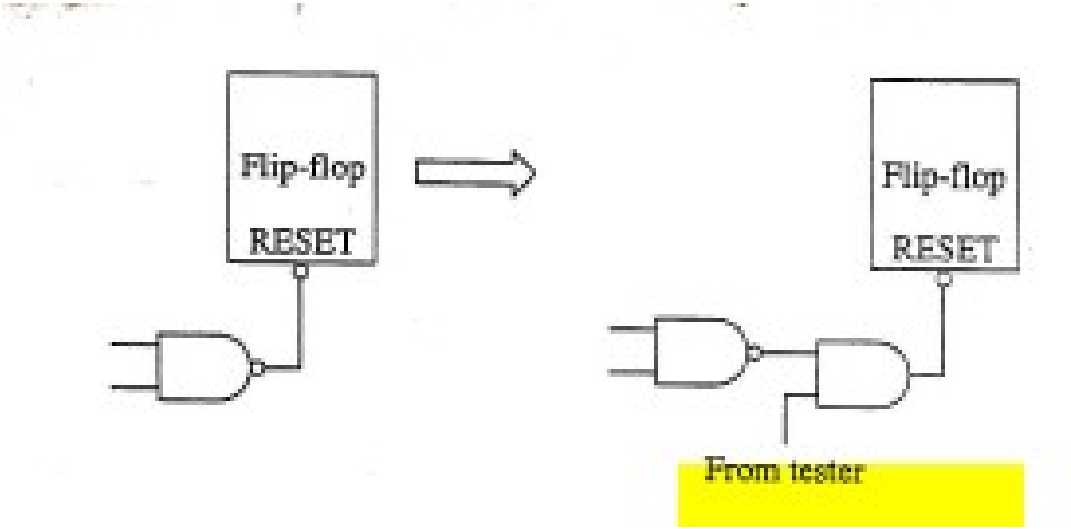
- Another approach to improve testability is to permit access to a subset of the Logic.
- Module B is physically embedded between two modules A and C.
- A set of gates G and H is inserted in to each of the input and outputs respectively, of module B..
- G, H functionality is Two input Mux and De-mux respectively
  - **Normal operation** – The test control signal is such that modules A, B and C are connected and the circuit performs the desired function.
  - **Test mode** – The test control input is changed, module B is connected to the primary inputs and outputs of the board. In this mode the control signal makes the outputs of module C as a high Impedance. So 'C' does not interfere with the test results generated by B
- This approach is similar to the technique of using multiplexers to improve testability.

To permit access to a subset of the Logic contd ..



Test state Registers

- The test mode signals required by the added hardware such as multiplexers, Tristate drivers etc cannot always be applied via the edge pins, because there are may not be enough of them.
- To overcome this problem, a Test state Register may be incorporated in the design.
  - This could be a shift register that is Loaded and Controlled by just a few signals.
  - The various testability hardware in the circuit can then be controlled by the parallel outputs of the shift register.
- Frequently, Flip-Flops, Counter, Shift Registers, and other Memory elements assume unpredictable states when power is applied, and they must be set to known states before testing can begin.
- Ideally, all memory elements should be reset from the external pins of the circuit, whereas in some cases additional logic may be required Figure.



Use of a multiplexer to simplify testing of long counter chains

- With complex circuits it may be desirable to set memory elements in several known states.
  - This allows independent initialization.
  - Also simplifies generation of certain internal states required to test the board adequately.
- A long counter chain presents another practical test problem.
  - Ex: The counter chain shown in Figure requires thousands of clock pulses to go through all the states.
- one way to avoid this problem is to break up the long chain into smaller ones by using a multiple
  - When
  - When

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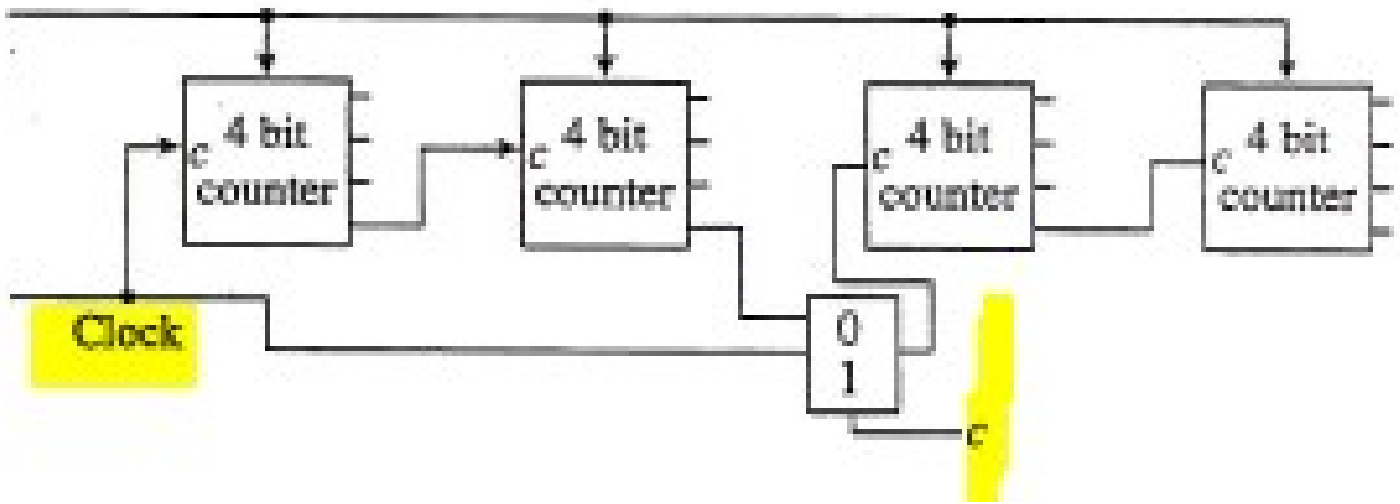
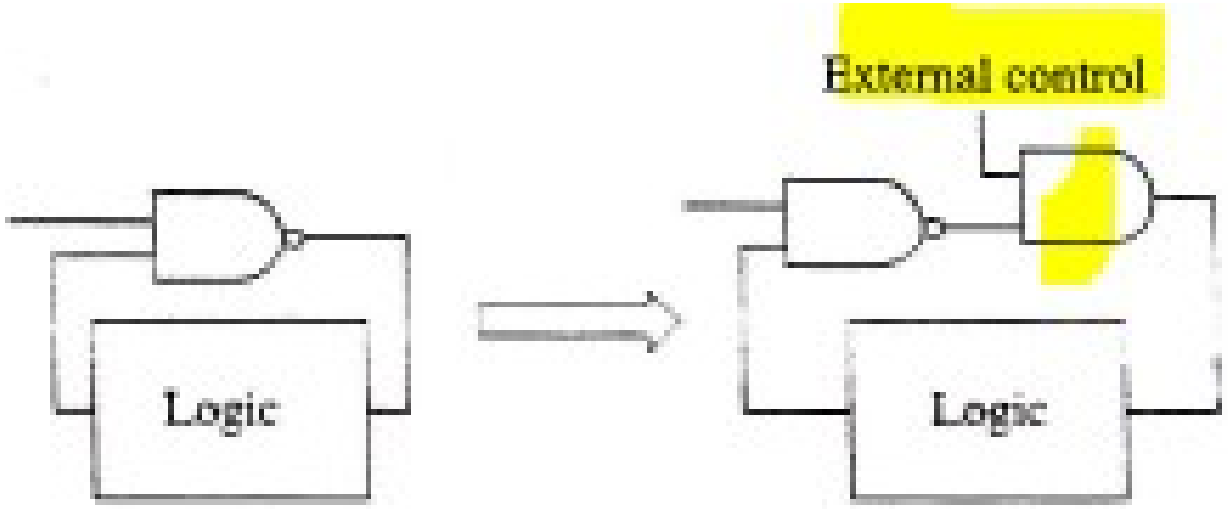


Breaking of feedback loop using an extra gate

- A feedback loop is difficult to test, because it hides the source of a fault. So, the feedback to be broken to test the fault by using one of the Two ways
  1. Breaking the loop physically To locate the fault of source.
     - Bringing both lines to external pins that can be short-circuited for normal operation.
     - when not short-circuited, the separated lines provide a control point and a test point.
  2. An alternative way of breaking a feedback, rather than using more costly test control points, is to add to the feedback path to a gate that can be interrupted by a signal from the tester .



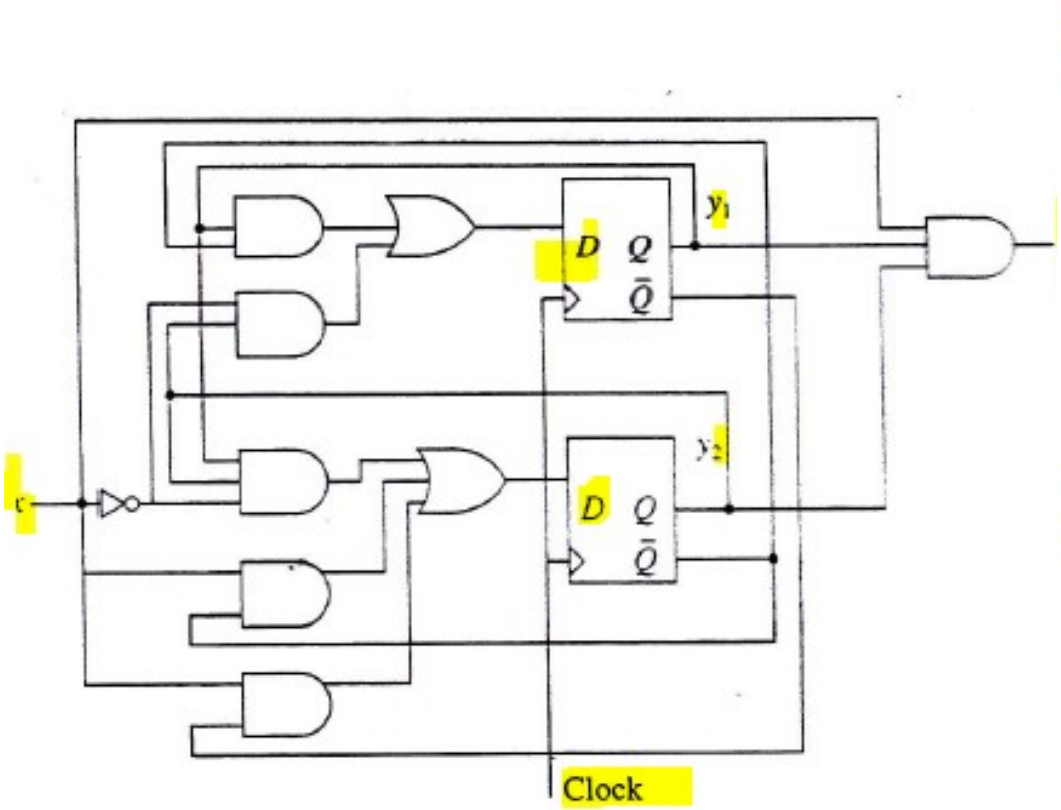
The Scan-Path Technique for Testable Sequential Circuit Design

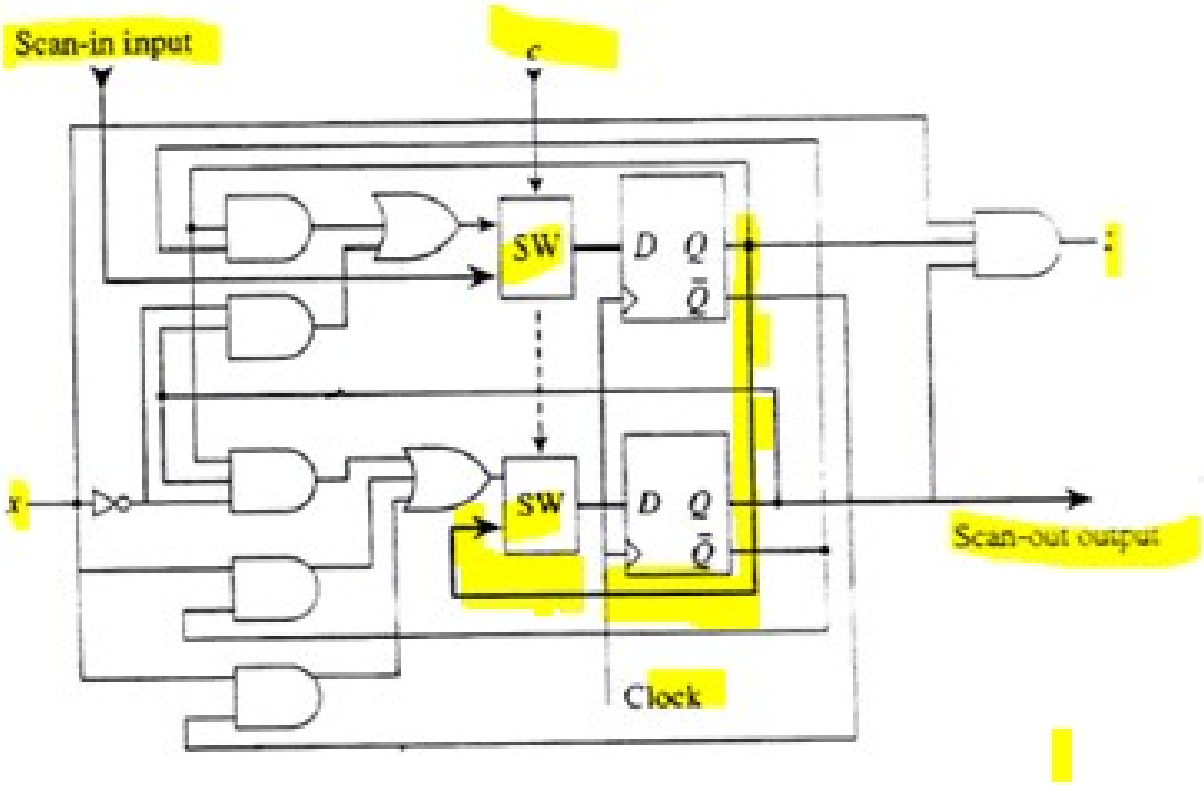
Scan-in for Sequential circuit

- The testing of sequential circuits is complicated because of the difficulties in setting and checking the states of the memory elements.
- These problems can be overcome by modifying the design of a general sequential circuit so that it will have the following two properties :
  1. The circuit can easily be set to any desired internal state.
  2. It is easy to find a sequence of input patterns such that the resulting output sequence will indicate the internal state of the circuit. In other words the circuit has a distinguishing sequence.
- The basic idea is to add an extra input ‘c’ to the memory excitation logic in order to control the mode of a circuit.
  - When c = 0 The circuit operates in its Normal mode
  - When c = 1 1 The circuit enters into a mode in which the elements are connected together to form a shift register.
  - This facility is incorporated by inserting a double-throw switch in each input lead of every memory element.

Scan-in for Sequential circuit

- These switches are grouped together and the circuit can operate either in it's normal mode / shift register mode. Figure –A shows a sequential circuit using D FFs;
- The modified circuit with Scan-in is shown in Figure B.

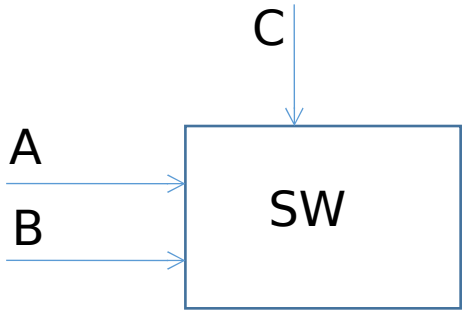


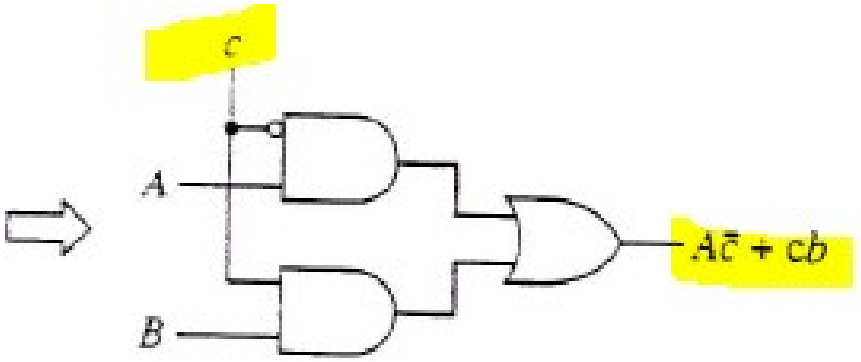


Realization of Double Throw Switch

- Double Throw Switch may be realized as shown below, where c is the control signal.

  Output A + CB





Procedure for testing the circuit

- One additional input connection to the modified circuit is required to supply the signal ‘c, to control all the switches.
- In the Shift Register mode First Flip-Flop can be set directly from the primary inputs (Scan-in inputs) and the output of the last Flip-Flop can be directly monitored on the primary output (Scan-out output).
- The circuit can be set to any desired state via the scan-out output.

- The procedure for testing the circuit is as follows:
  1. Set c = 1 to switch the circuit to Shift Register mode.
  2. check operation as a Shift Register by using scan-in inputs, scan-out output and the clock.
  3. Set the initial state of the shift register.
  4. Set c = 0 to return to the normal mode.
  5. Apply test input pattern to the combinational logic.
  6. Set c = I to return to shift register mode.
  7. Shift out the final state while setting the starting state for the next test.
  8. Go to step 4.

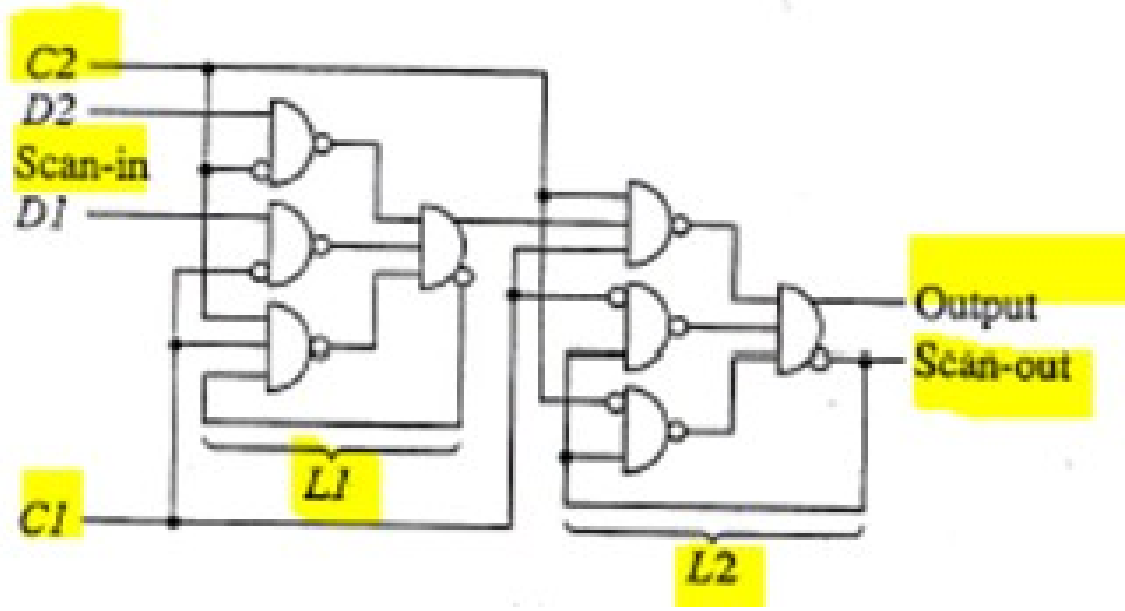
Scan Path Technique

- With this procedure (Scan Path Technique) , a considerable proportion of the actual testing time is spent in setting the state.
- An operation that requires a number of clock pulses equal to the length of the shift register.
- This time may be decreased by forming several short Shift Registers rather than a single Long one;
- The time needed to set or read the state = the Length of the longest Shift Register.
- The extent to which the number of Shift Registers can be increased is determined by the number of input and output connections available to be used to drive and sense the shift registers.

- Advantage of the scan-path approach:
  1. A sequential circuit can be transformed into a combinational circuit, thus making test generation for the circuit relatively easy.
  2. Very few extra gates or pins are required for this Transformation.

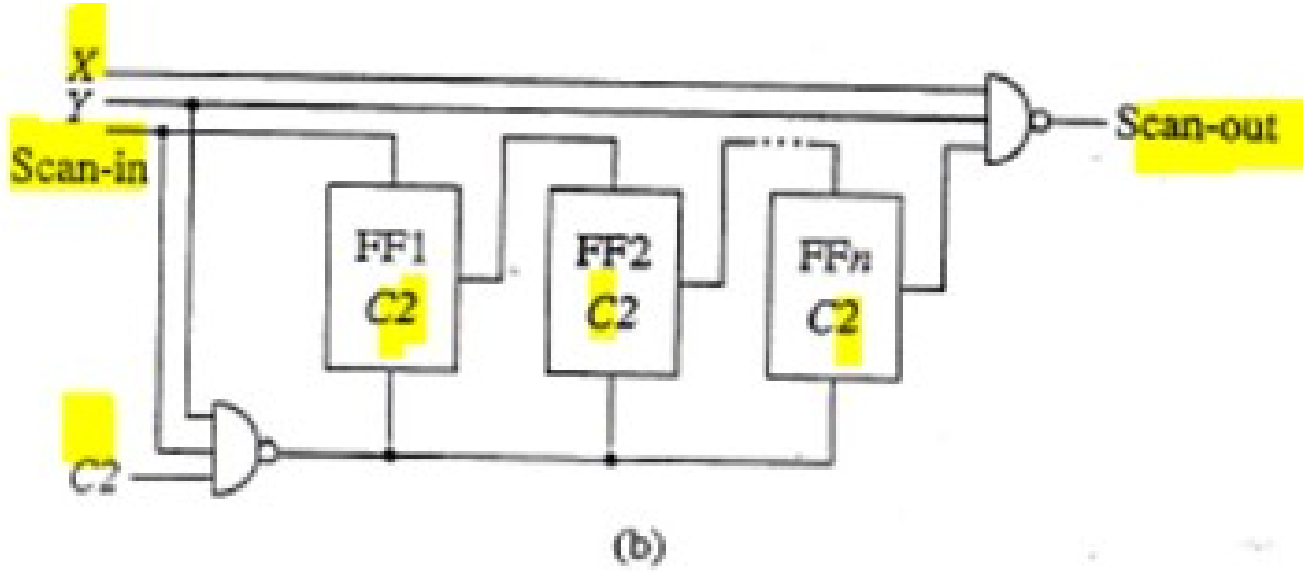
Scan-path technique with Race less D-type Flip-Flop

- The basic memory element used in this approach is known as a Race less D-type Flip-Flop with scan path Figure) shows such a memory element, which consists of two latches L1 and,L2.
- C1 , C2 are Clock signals. D1 → Data ; D2 → Test data
- Normal operation : when C1 = 0 ; C2 = 1 for sufficient time to latch up the data at input D1. (Data Latch)
  - when C1 = 1 → The output of L1 is latched into L2.
- Scan-in operation : when C2= 0 → by clocking the test input value at D2 into the latch L1. (Test input Latch)
  - when C2 = 1 → The output of the L1 latch is clocked into L2.



Scan-Path approach used at logic card level

- The configuration of the scan-path approach used at logic card level is shown in Figure (b).
- X-Y Address Signals
- All the Flip-Flops on a logic card are connected as a Shift Register, such that for each card there is one scan path.
- There is provision for selecting a specified card in a subsystem.
- If a card is not selected, its output is blocked; thus, a number of card outputs in a sub-system can be put together with only a particular card having control of the test output for that subsystem.



(b)

Equivalence Checking

Benefits:

- Equivalence checking provides a powerful addition to any design flow.
- The ability to apply formal methods to verify the consistency of a design gives insight into the quality of the result that is not dependent on the completeness of the test bench. Specific benefits include:
  - **Higher efficiency.** Less reliance on slower gate-level simulation.
  - **Higher confidence.** Less concerns that the tool chain or ECOs have introduced subtle errors.
  - **Higher quality.** This technique can highlight poor RTL coding in the design.
  - **Higher predictability.** Less chance of missing bugs.
- Logic equivalence checking (LEC) Looks at the combinatorial structure of the design to determine if the structure of two alternative implementations will exhibit the same behavior. If operations such as retiming are applied to a design, the structure of the design will no long map between the two representations.
- Sequence equivalency checking (SEC) Takes timing into account and examines the equivalency of two design representations over multiple clock cycles.

Ref:

https://www.synopsys.com/glossary/what-is-equivalence-checking.html#:~:text=Logic%20equivalence%20checking%20(LEC)%20looks,map%20between%20the%20two%20representations